1 SPECIFICATION

1.1 DESCRIPTION

- Halogen Free
- 125°C maximum total temperature operation
- 2.7 x 2.2 x 1.2mm maximum surface mount package
- Magnetically shielded, low EMI
- High current carrying capacity, Low core losses
- RoHS compliant

1.2 APPLICATIONS

- Voltage Regulator Module (VRM)
- Multi-phase regulators
- Point-of-load modules
- Smart phone POL modules
- SSD modules
- Notebook regulators
- Battery power systems
- Graphics cards
- Data networking and storage systems
- DC/DC converter
- Cellular phones, LCD displays, HDDs
- Thin type on-board power supply module for exchanger

1.3 ENVIRONMENTAL DATA

- Storage temperature range: -55°C to +125 °C
- Operating temperature range: -55°C to +125°C (ambient plus self-temperature rise)
- Solder reflow temperature: J-STD-020D compliant

1.4 PRODUCT IDENTIFICATION

CPLB-252012-R33-M

(1) (2) (3) (4)

(1)Product Series

(2)Choke Size

(3)Initial Inductance(L @ 0A):R33=0.33μH

(4)Inductance Tolerance:M=L+/-20%

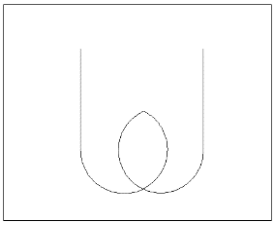
1.5 ELECTRICAL PARAMETERS

Part Number	L0 (μH) ±20%	IDC (Amp) Max.	IDC (Amp) Typ.	ISAT (Amp) Max.	ISAT (Amp) Typ.	DCR (mΩ) Typ. @25℃	DCR (mΩ) Max. @25℃
CPLB-252012-R33-M	0.33	5.1	6.0	7.6	8.5	14.0	19.0
CPLB-252012-R47-M	0.47	5.5	6.1	6.7	7.3	17.0	21.0
CPLB-252012-R68-M	0.68	5.0	5.5	6.0	6.3	25.0	30.0
CPLB-252012-1R0-M	1.0	3.9	4.2	5.0	5.4	35.0	42.0
CPLB-252012-1R5-M	1.5	3.2	3.6	3.4	3.6	53.0	61.0
CPLB-252012-2R2-M	2.2	2.7	3.0	3.0	3.3	68.0	82.0
CPLB-252012-3R3-M	3.3	1.8	2.1	2.5	2.8	110.0	135.0
CPLB-252012-4R7-M	4.7	1.5	1.8	2.1	2.4	160.0	190.0

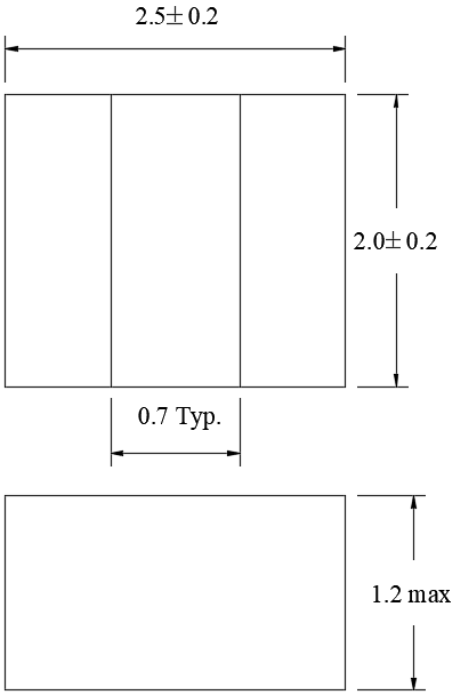
Notes:

1. Initial Inductance (L_0) Test Parameters:1MHz,1V,Idc=0.0A,+25℃
2. Operating temperature range - 55 °C to + 125 °C
3. I_{DC}(A):DC current (A) that will cause an approximate ΔT of 40 °C
4. I_{SA}T(A):DC current (A) that will cause L0 to drop approximately 30 %
5. The part temperature (ambient + temp rise) should not exceed 125 °C under worst case operating conditions. Circuit design, component placement, PWB trace size and thickness, airflow and other cooling provisions all affect the part temperature. Part temperature should be verified in the end application.
6. The rated current as listed is either the saturation current or the heating current depending on which value is lower.

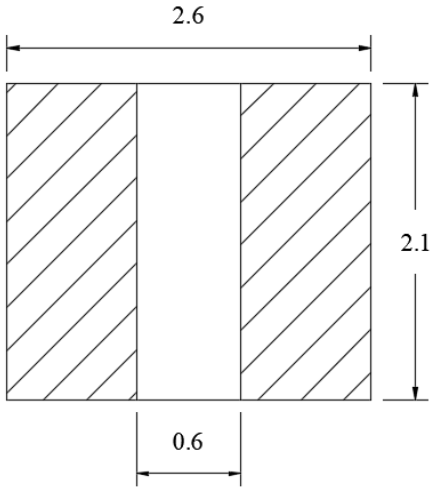
1.6 Schematics



1.7 MECHANICAL PARAMETERS



1.8 RECOMMENDED PCB LAYOUT

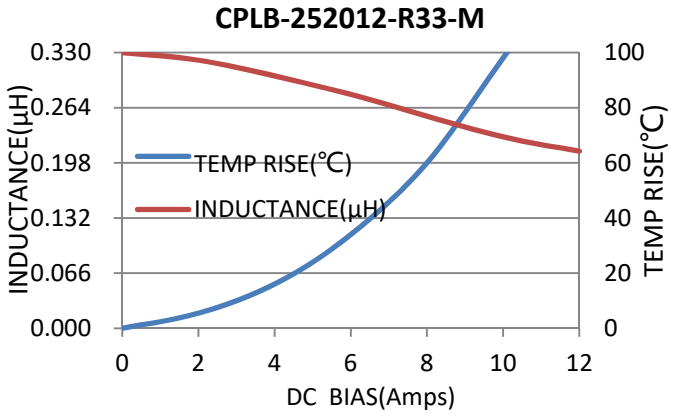


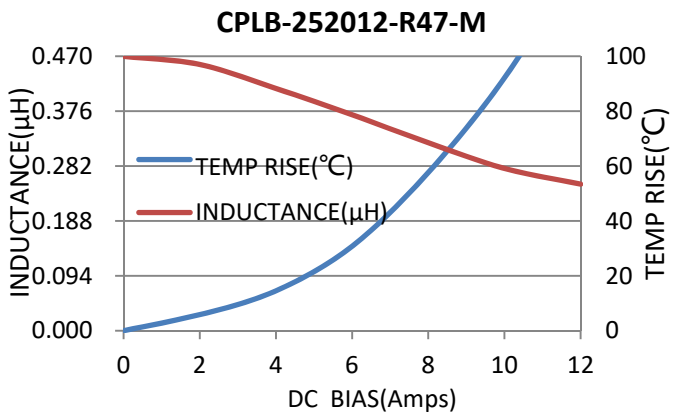
(unit:mm)

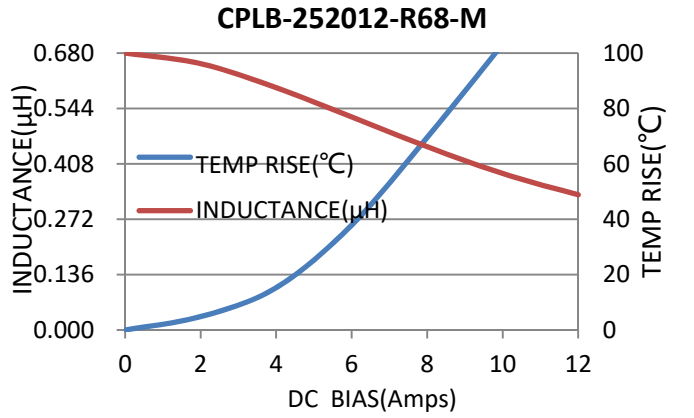
Notes:

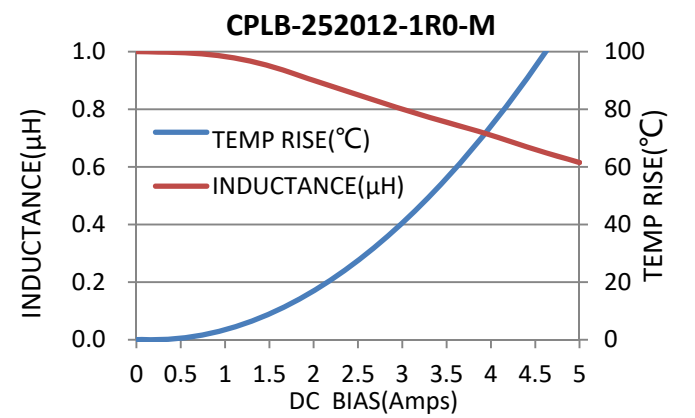
1. Tolerances are +/-0.1millimeters unless stated otherwise
2. Dimensions of recommended PCB layout are reference only.
3. Do not route traces nor place vias underneath the inductor. Proper layout is required.

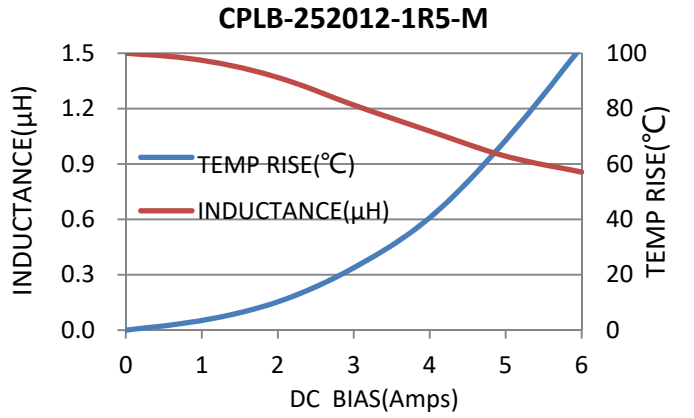
2 INDUCTANCE & TEMPERATURE RISE VS IDC

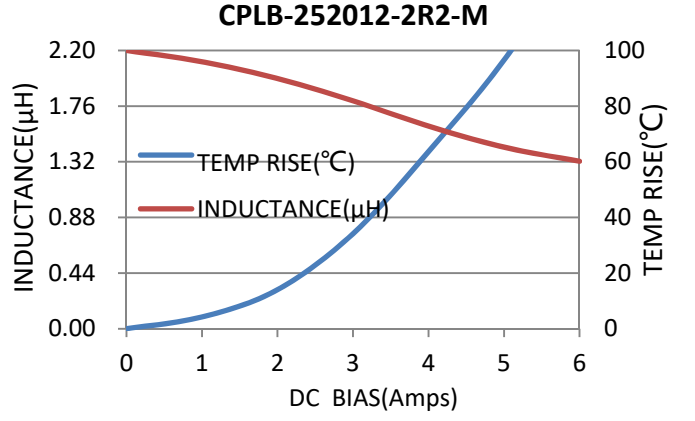


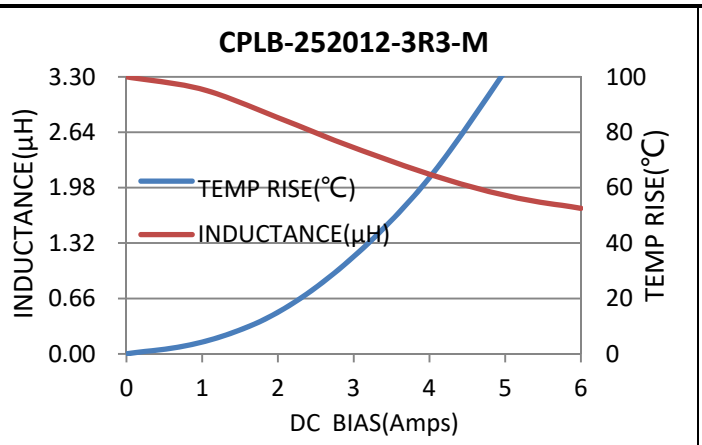


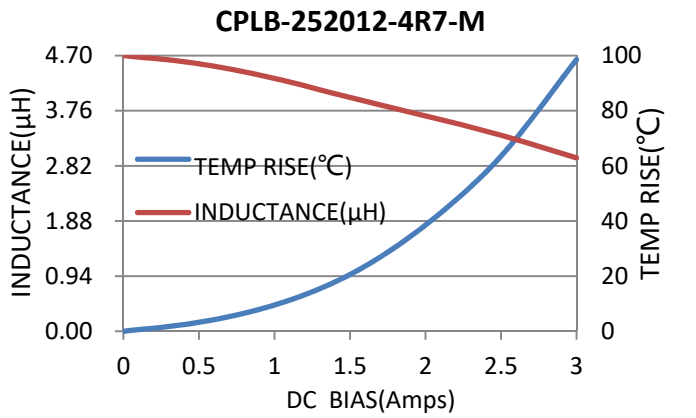












3 REFLOW PROFILE

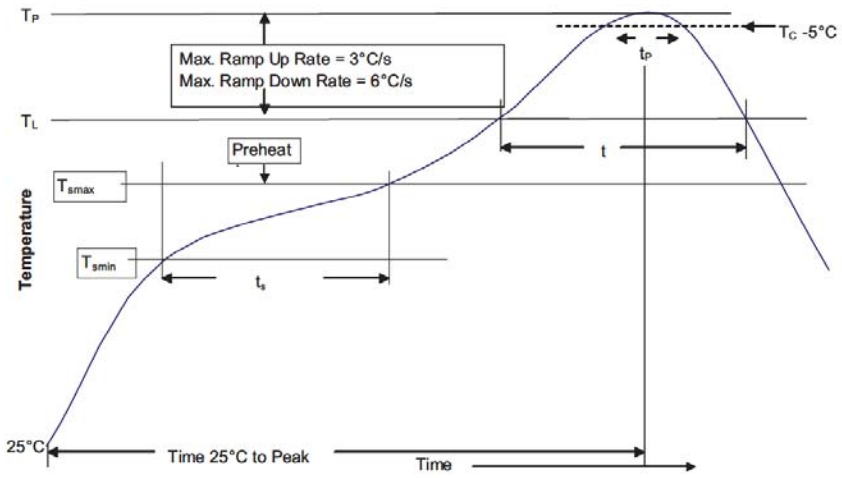


Table 1 - Standard SnPb Solder (T_C)

Package Thickness	Volume mm3 <350	Volume mm3 ≥350
<2.5mm)	235°C	220°C
≥2.5mm	220°C	220°C

Table 2 - Lead (Pb) Free Solder (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ 350 - 2000	Volume mm³ >2000
<1.6mm	260°C	260°C	260°C
1.6 – 2.5mm	260°C	250°C	245°C
>2.5mm	250°C	245°C	245°C

Reference JDEC J-STD-020

Profile Feature		Standard SnPb Solder	Lead (Pb) Free Solder
Preheat and Soak	• Temperature min. (T_{smin})	100°C	150°C
	• Temperature max. (T_{smax})	150°C	200°C
	• Time (T_{smin} to T_{smax}) (t_s)	60-120 Seconds	60-120 Seconds
Average ramp up rate T_{smax} to T_p		3°C/ Second Max.	3°C/ Second Max.
Liquidous temperature (T_L) Time at liquidous (t_L)		183°C 60-150 Seconds	217°C 60-150 Seconds
Peak package body temperature (T_P)*		Table 1	Table 2
Time (t_p)** within 5 °C of the specified classification temperature (T_C)		20 Seconds**	30 Seconds**
Average ramp-down rate (T_p to T_{smax})		6°C/ Second Max.	6°C/ Second Max.
Time 25°C to Peak Temperature		6 Minutes Max.	8 Minutes Max.

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.